WEST Search History

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Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L28	(L15 or L23 or nop or noop or no-op) same reorder buffer$1	2
		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
☐	L27	(L19 or L26 or nop or noop or no-op) and reorder buffer$1	0
☐	L26	("no operation" or "no-operation")	1655
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L25	(L19 or L23 or nop or noop or no-op) same reorder buffer$1	2
☐	L24	(L19 or L23 or nop or noop or no-op) with reorder buffer$1	1
☐	L23	("no operation" or "no-operation")	11441
☐	L22	nop with compress$3	48
		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
☐	L21	nop with compress$3	8
☐	L20	L19 adj (flag$1 or indicator$1)	0
☐	L19	"non operation" or "non-operation"	3781
☐	L18	("no operation" or "no-operation") adj (flag$1 or indicator$1)	0
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L17	("no operation" or "no-operation") adj (flag$1 or indicator$1)	6
☐	L16	L15 adj (flag$1 or indicator$1)	6
☐	L15	"non operation" or "non-operation"	3949
☐	L14	buffer$1 with L13	9
☐	L13	nop with flag$1	139
☐	L12	nop with indicator$1	15
		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
☐	L11	nop with indicator$1	2
☐	L10	nop with flag$1	11
☐	L9	L7 or L8	3
☐	L8	nop indicator$1	1
☐	L7	nop flag$1	2
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L6	nop flag$1	18
☐	L5	nop indicator$1	2
☐	L4	fold$3 with nop	9

☐	L3	l1 with L2	148
☐	L2	onchip or on-chip	28153
☐	L1	dram with cache	4143

END OF SEARCH HISTORY

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Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, I CNF = IEE Conference, IEEE STD = IEEE Standard

1. **The cache DRAM architecture: a DRAM with an on-chip cache memory**
   Hidaka, H.; Matsuda, Y.; Asakura, M.; Fujishima, K.;
   Micro, IEEE
   Volume 10, Issue 2, April 1990 Page(s):14 - 25
   IEEE JNL

2. **An experimental 1-Mbit cache DRAM with ECC**
   Asakura, M.; Matsuda, Y.; Hidaka, H.; Tanaka, Y.; Fujishima, K.;
   Solid-State Circuits, IEEE Journal of
   Volume 25, Issue 1, Feb. 1990 Page(s):5 - 10
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3. **A circuit design of intelligent cache DRAM with automatic write-back capability**
   Arimoto, K.; Asakura, M.; Hidaka, H.; Matsuda, Y.; Fujishama, K.;
   Solid-State Circuits, IEEE Journal of
   Volume 26, Issue 4, April 1991 Page(s):560 - 565
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4. **An eyperimental 1Mb cache DRAM with ECC**
   Asakura, M.; Matsuda, Y.; Hidaka, H.; Tanaka, Y.; Fujishima, K.; Yoshihara, T.;
   VLSI Circuits, 1989. Digest of Technical Papers., 1989 Symposium on
   1989 Page(s):43 - 44
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